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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/343,872	06/30/1999	TUAN Q. DAO	5201-20400	8423

24319 7590 08/24/2004

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EXAMINER	
HUYNH, KIM T	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/343,872	DAO ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 10-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-8, 10-12, 14-17, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (Pub No US20020002662) in view of Pascucci (US Patent 5,815,457) and further in view of Ryan (Pub No US20020161965)

As per claim 1, Olarig discloses a data transfer apparatus that comprises:

- A first bus lines configured to transfer data bits between a first processing device and a corresponding first memory module;[0134-0136]
- A second bus lines configured to transfer data bits between a second processing device and a corresponding second memory module;[0134-0136]
- Group of cross-bus lines configured to transfer data bits between the first bus lines and the second bus lines via bus bridges; and [0134-0138]
- A memory management unit configured to receive memory access requests from the first and second processing devices and to

responsively configure the bus bridges to steer address and data signals accordingly,[0013],[0040]

Olarig discloses all the limitations as above except group of bus lines. However, Pascucci discloses a bit line selection decoder for memory having a plurality of bit lines in a plurality of groups. Each switch for selecting one of the plurality of bit lines in response to a control signal from a set of control lines applied to each group of bit lines. (col.1, line 60-col.3, line 7)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Pascucci's teaching into Olarig's system so as to reduce the number of control lines that activate individual bit lines. (col.1, lines 44-47)

Furthermore, Olarig fails to teach wherein group of bus lines includes two unidirectional bit lines for each data bit and wherein the bus bridges include a multiplexer for each outgoing bit line that selects from the three other incoming bit lines. However, Ryan discloses memory controller communicates commands and addresses to C/A bus which is a unidirectional bus. C/A is coupled to the plurality of memory devices. C/A receives and latches the command and address information from C/A bus and connected to data bus and memory modules. [0038-0039]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ryan'

teaching into Olarig's system so as to support increased bandwidth.[0007]

As per claim 11, Olarig discloses a method for transferring data between a set of memory modules and a set of processor units, wherein the method comprises:

- Said processing units providing transfer requests to a memory manager; [0040]
- Said memory manager setting a router in a conflict-free access pattern in response to said transfer requests, wherein setting said router includes; [0137], [0142]
- Said memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between the local busses, [0134-0137]
- Wherein the local busses each include two bit lines for each data bit and the cross-bus includes two bit lines for each data bit, wherein the bus bridges each include a multiplexer for each outgoing bit line that selects from multiple incoming bit lines; and [0074-0076]
- Said processing units accessing memory modules via said router. [0136-138]

Olarig discloses all the limitations as above except wherein the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses each includes two

unidirectional bit lines for each data bit. However, Ryan discloses memory controller communicates commands and addresses to C/A bus which is a unidirectional bus. C/A is coupled to the plurality of memory devices. C/A receives and latches the command and address information from C/A bus and connected to data bus and memory modules. [0038-0039]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ryan' teaching into Olarig's system so as to support increased bandwidth.[0007]

As per claim 15, Olarig discloses a high-bandwidth bus which comprises

- A plurality of local busses each for transferring data between a processing device and an associated memory module;[0136-0138]
- A cross-bus for transferring data among the plurality of local busses, wherein said cross-bus is coupled to each of the plurality of local busses by a bridge means; and [0134-138]
- A memory controller 200 means for setting said bridge means to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules; [0142]

Olarig discloses all the limitations as above except group of bus lines. However, Pascucci discloses a bit line selection decoder

for memory having a plurality of bit lines in a plurality of groups. Each switch for selecting one of the plurality of bit lines in response to a control signal from a set of control lines applied to each group of bit lines. (col.1, line 60-col.3, line 7)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Pascucci's teaching into Olarig's system so as to reduce the number of control lines that activate individual bit lines. (col.1, lines 44-47)

Furthermore, Olarig fails to teach wherein the local buss line groups each include oppositely configured unidirectional bit lines for each data bit and the cross-bus lines includes oppositely configured unidirectional bit lines for each data bit; and a bridge means that includes bi-directional data channel bridges and unidirectional address channel bridges. However, Ryan discloses an improved memory system is provides having a unidirectional command and address bus coupled to a memory controller, the memory controller communicating commands and addresses to the command and address bus. A bi-directional data bus is also coupled to the memory controller, the memory controller communicating data information to the bi-directional data bus for a write operation and receiving the data information from the bidirectional data bus during a read command[0008] and furthermore, memory controller communicates commands and addresses to C/A bus which is a

unidirectional bus while data bus is a bi-directional bus. C/A is coupled to the plurality of memory devices. C/A receives and latches the command and address information from C/A bus and connected to data bus and memory modules. [0038-0039]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ryan' teaching into Olarig's system so as to support increased bandwidth.[0007]

As per claim 16, Olarig discloses a high-bandwidth bus system which comprises:

- A plurality of local memory busses each for transferring data between a processing device and an associated memory module;[0136-0138]
- One or more local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection and wherein the local intersect busses are segmented with latches to allow multiple data signals to be transmitted concurrently via the local intersect busses; and [0134-0138], [0139]
- A memory controller 200 means for setting each multiplexer to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide

highest priority for accesses from processing devices to the associated memory modules, [142]

Olarig discloses all the limitations as above except wherein the local memory busses each include two unidirectional bit lines for each data bit and the local intersect busses each includes two unidirectional bit lines for each data bit. However, Ryan discloses memory controller communicates commands and addresses to C/A bus which is a unidirectional bus. C/A is coupled to the plurality of memory devices. C/A receives and latches the command and address information from C/A bus and connected to data bus and memory modules. [0038-0039]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Ryan' teaching into Olarig's system so as to support increased bandwidth.[0007]

As per claim 3, Olarig discloses wherein the memory management unit includes an interrupt controller 190 configurable to assert an interrupt signal to said processing devices after completing a block transfer of data. [0137-139]

As per claims, 4-6, 14, 19-22, Olarig discloses wherein the memory management unit includes one or more request queues, wherein said one or more request queues includes a single transfer queue configured to store access requests relating to single data word, block data, message

transfers [0142], [0013], wherein identify requests, ie memory access parameters inherently discloses type of data transfer)

As per claims 7, 23, Olarig discloses wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to a processing device that is an addressee of a message transfer request. [0137-0138]

As per claims 8, 24, Olarig discloses the data transfer further comprising port logic connected to the first and second groups of bus lines and configured to couple to the processing devices, wherein the port logic is further coupled to the memory management unit and configured to prevent writes to protected memory. [0074-0076]

As per claim 10, Olarig discloses wherein each group of bus lines includes at least three unidirectional bit lines. [0134-0136]

As per claim 12, Olarig discloses wherein before setting said router, said memory manager determines said conflict-free access pattern in accordance with assigned priorities for each transfer request. [0142]

As per claim 17, Olarig discloses wherein the four multiplexers forward data between a processing device and a memory device with essentially no latency delay.[0142]

As per claim 25, Olarig discloses a system, comprising:

- A plurality of processors;(fig.9, 102a-h)
- A plurality of memory modules, each memory module being coupled to and paired with one of the processors via separate bus

lines such that a data read requested from processor to a paired memory module is received on a first clock cycle subsequent to a clock cycle that provides an address;[0138-0139]

- A segmented cross-bus lines that couple to the separate bus lines using buffers such that multiple data signals are simultaneously transferable between the bus lines via the cross-bus lines,[0134-139]
- Wherein the cross-bus lines are configurable to latch signals to the separate sets of bus lines such that throughput and cross-path latency between processors and memories that are not paired is customizable.[0138-0139]

Olarig discloses all the limitations as above except group of bus lines. However, Pascucci discloses a bit line selection decoder for memory having a plurality of bit lines in a plurality of groups. Each switch for selecting one of the plurality of bit lines in response to a control signal from a control lines applied to each group of bit lines. (col.1, line 60-col.3, line 7)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Pascucci's teaching into Olarig's system so as to reduce the number of control lines that activate individual bit lines. (col.1, lines 44-47)

3. Claims 2, 13,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (Pub No US20020002662) in view of Pascucci (US Patent 5,815,457) and further in view of Ryan (Pub No US20020161965) and further in view of Geiger et al. (Pub No US20020091905)

Olarig discloses all the limitations as above except memory manager operating a direct memory access controller to perform data transferring between memory modules. Whereas, Geiger discloses system 200 is operable to data transferred to/from memory components or devices comprises on the module include DMA controller to move data in the system memory. [0122]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Geiger's teaching into Olarig's system so as to have ability to access transferred data independently between modules.

4. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (Pub No US20020002662) in view of Pascucci (US Patent 5,815,457) and further in view of Ryan (Pub No US20020161965) and further in view of Prasad et al. (US Patent 6,275,491)

Olarig discloses all the limitations as above except wherein at least two sets of the bus lines have different widths. However, Prasad discloses each data buses includes multiple groups of lines, each group dedicated to an associated one of port processors with the width of each group determined according to the data path width to be switched in each cycle. (col.5, lines 14-30)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Prasad's teaching into Olarig's system so as to reduce the I/O burden on the switch fabric. (col.3, lines 32-38)

Response to Amendment

5. Applicant's amendment filed on 5/5/04 have been fully considered but are moot in view of the new ground(s) of rejection.

a. In response to applicant's argument that Olarig does not teach or suggest a first group bus lines and a second group of bus lines. However, Pascucci discloses a bit line selection decoder for memory having a plurality of bit lines in a plurality of groups. Each switch for selecting one of the plurality of bit lines in response to a control signal from a set of control lines applied to each group of bit lines. (col.1, line 60-col.3, line 7)

b. In response to applicant's argument that Olarig does not teach or suggest bi-directional data channel bridges and uni-directional address channel bridge. However, Ryan discloses an improved memory system is provides having a unidirectional command and address bus coupled to a memory controller, the memory controller communicating commands and addresses to the command and address bus. A bi-directional data bus is also coupled to the memory controller, the memory controller communicating data information to the bi-directional data bus for a write operation and receiving the data information from the bi-directional data bus during a read command[0008] and furthermore, memory controller communicates commands and addresses to C/A bus which is a unidirectional bus while data bus is a bi-directional bus. C/A is coupled to the

plurality of memory devices. C/A receives and latches the command and address information from C/A bus and connected to data bus and memory modules. [0038-0039]

Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM-6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

August 7, 2004

MARK H. RINEHART
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